FMI Applied to the Study of the Temperature Distribution in Flip Chips

N. Boyer[1,2], D. P. Masson[1], M. Meunier[2], M. Simard-Normandin[1]

Nortel Networks[1]
Centre for Microanalysis
185 Corkstown Road, Dept. P965
Nepean, ON. Canada

Ecole Polytechnique[2]
2900, Boul. Edouard-Montpetit
Montreal, QUÉ. Canada H3C 3A7

email: *nicolas.boyer.P965stu@nt.com*

Abstract

The use of fluorescent microthermal imaging (FMI) as a tool to study the temperature distribution in flip chip packages was investigated. Backgrinding of the die was required to minimize heat diffusion and maximize the spatial resolution. A test structure was created in order to evaluate the spatial resolution of FMI from the backside of flip chips as a function of the die thickness and of the power dissipation. A lateral resolution of 50 μm is obtained after polishing the die to a thickness of 5 μm. At this thickness, the centre of a hot spot can be located with a precision of ± 5μm. For a 5 μm thick die, the FMI temperature map revealed the heat-sinking effect of the flip chip's solder bumps.

I. Introduction

Flip Chip on Board (FCOB) assembly technology offers small size, light weight and high pin count integrated circuit packages. This low cost technology also allows the reduction of interconnect inductance. Thus, the flip chip technology offers a unique packaging solution for portable and personal communication equipment [1]. FCOB structures will soon be widespread in the microelectronic industry.

The growing popularity of FCOB in the industry has forced the development of new analysis tools and techniques to support the development and the production of FCOB devices.

Fluorescent microthermal imaging (FMI) was developed to find failure sites and to obtain temperature profiles over the surface of integrated circuits [2,3,4,5]. In this work, the application of this technique to the analysis of FCOB structures for failure and reliability analyses has been investigated. Particularly, the spatial resolution of the technique for different silicon die thicknesses has been studied.

A. *Flip Chip Technology*

In conventional packages, the semiconductor die is glued to a copper support pad before encapsulation. The copper pad gives mechanical stability to the device and serves as a heat sink. For a FCOB, the back of the die is bare and exposed, and the heat from the circuit is dissipated through the solder bumps via the board metallization [6]. Figure 1 illustrates the cross-section of a FCOB structure.

It is possible to open or decapsulate a conventional package using fuming acids and to observe directly the temperature profile at the circuitry's surface. For FCOB, the circuitry is hidden between the Si die and the epoxy underfill. As shown in this work, FMI temperature profiles can be obtained from the back surface of the Si die. However, the image resolution is compromised by the heat diffusion through the Si.

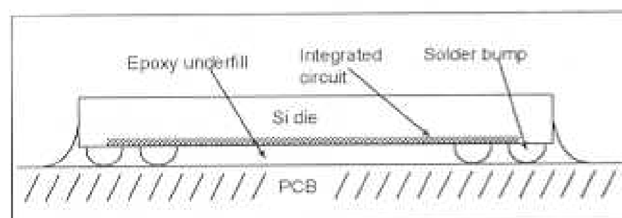


Figure 1. Cross-section view of a FCOB. Failure analysis of such a circuit is difficult because the circuitry is hidden between the Si die and the underfill material.

B. *Fluorescent Microthermal Imaging*

Successful fluorescent microthermal imaging was first demonstrated by Tyson and Kolodner [2,3]. FMI relies on the temperature dependent fluorescent yield of a europium chelate: EuTTA (Europium thenoyltrifluoroacetonate). The EuTTA fluoresces at 612 nm when excited by UV light at 365 nm. The fluorescence intensity is inversely proportional to the temperature. This technique was described in detail by Barton et *al.* [4,5].

In a typical FMI experiment, two fluorescence images are captured: one at room temperature and the other when the chip is powered up. The ratio of the intensities of the two images reveals changes in temperature over the IC surface.

II. Experimental

FMI was implemented on a Zeiss laser scanning microscope (LSM). A mercury arc lamp provides the excitation energy required by the EuTTA molecules to fluoresce. A liquid-cooled CCD is used to detect the fluorescence. A narrow band filter centered at 612 nm allows only the EuTTA fluorescence to be captured.

A. *Film deposition*

The EuTTA powder was mixed with PMMA in chlorobenzene in proportions (% weight) of 1.2:1.8:97. The highest uniformity was obtained by immersion of the die under a big drop of the EuTTA solution. The drop was allowed to dry and cure in an oven at 100^0C for one hour. Film thicknesses ranging from 200 to 500 nm were obtained. This evaluation is based on thickness measurements obtained from a profilometer and from the observation of interference fringes using Fourier Transform Infrared spectroscopy (FTIR). All films were exposed to UV light (using the 5X lens) for 10 minutes prior to image acquisitions. This reduces the spatial artefacts arising from the bleaching of the film. Bleaching refers to the reduction of the fluorescence of the film as a function of the UV exposure. The spatial

artefacts observed in FMI are due mainly to the dependence of the bleaching on the film thickness [7].

B. *Test structure preparation*

A chip consisting of 3 μm wide Al lines covered by passivation layers was modified to create a suitable test structure. The area of interest is shown in Figure 2. The gray pattern represents the unused part of the test device circuitry. The current path on Figure 2 is shown by the arrows on the black lines. The horizontal black line on Figure 2 is actually made of two parallel Al lines (too close to be distinguished), separated by 2 μm, where current flows in opposite directions. These two metal lines turn downward at point

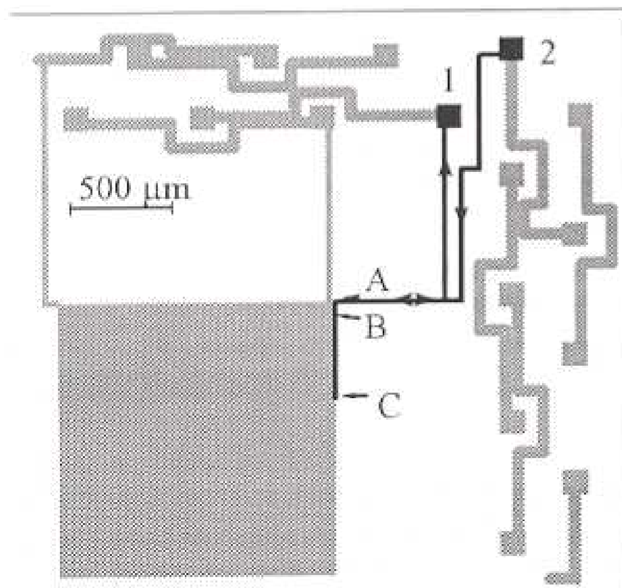


Figure 2. Modified test chip. Bridges A, B and C were made to short-circuit the two metal lines connected to bumps 1 and 2. Current flows through the circuit shown in black isolated from the rest of the original circuitry (gray). Bridges B and C were, respectively, 40 and 400 μm away from bridge A.

A towards points B and C. Bridges were made at point A, B and C as shown in Figure 3. The deposition of tungsten to short-circuit the lines was performed using a focused ion beam (FIB).

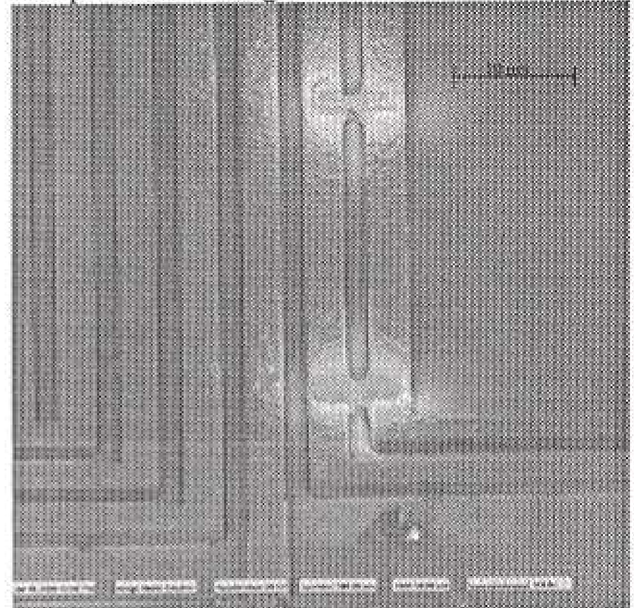


Figure 3. SEM image of the tungsten bridges A and B deposited with FIB microsurgery. The tungsten lines are 3 micrometers wide.

Alignment of the die with the PCB board, reflow and underfilling were subsequently done to form the final FCOB test structure.

Preliminary results obtained from the backside of a 400 μm thick die didn't reveal any details. Only a uniform overall heating of the die was observed. Backgrinding was therefore needed to unveil the details of the test structure and to evaluate the technique's spatial resolution. Polishing was done using a standard sample preparation polisher for electron microscopy.

FMI measurements were done for 7 different die thicknesses ranging from 250 to 5 micrometers. Die thicknesses above 40 μm were measured by focusing the image from an infrared laser beam (λ=1152 nm) on the circuitry and then on the back of the Si die surface. The thickness is obtained by multiplying this distance by the index of

refraction of Si at this wavelength. For less than 40 μm, thicknesses were obtained from the multiple reflection fringes seen in the IR spectrum of the films.

III. Results and Discussion

The temperature profiles observed for die thicknesses ranging from 5 to 150 micrometers are shown in Figure 4. They were acquired using the 5X lens. The features of the layout are distinguishable for thicknesses less than 100 μm only. The positions of bridges A, B and C are pointed on Figure 4c). On these pictures however, bridges A and B are not resolved. They are distinguishable, at higher magnification, for the thinnest sample only.

Bridge C was not observed because of its lower energy dissipation. The location of the three bridges is shown on Figure 4c). For a die thickness of 150 μm we estimate the spatial resolution to be of the order of 250 μm. For the thinnest die, 5 μm, the resolution is about 40 μm. Note however that the centroid of the object can be located with a precision of about 5 μm at a thickness of 5 μm.

The temperature profile along the line shown in Figure 4c) is illustrated in Figure 5. The temperature drops down faster on the left side of the curve corresponding to the lower half region on Figure 4c).

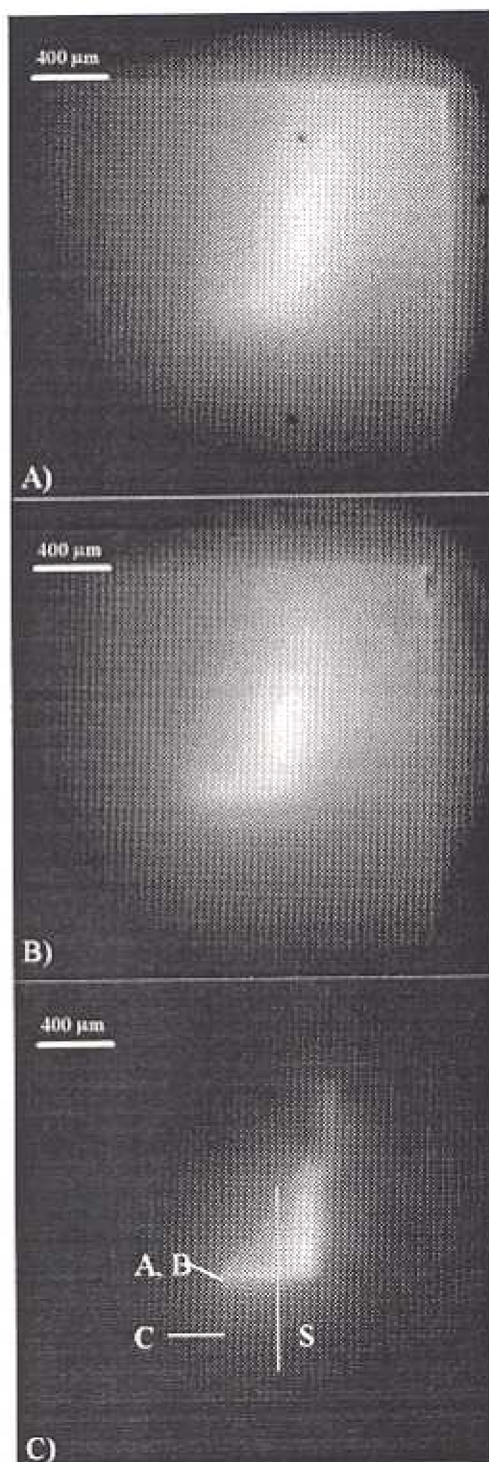
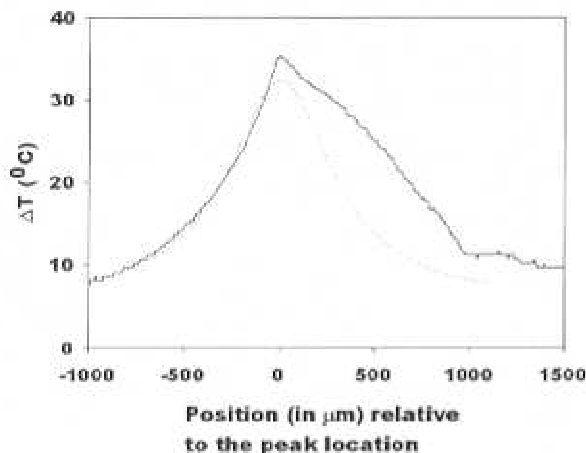


Figure 4. Thermal profiles for thicknesses of 150 μm (a), 70 μm (b) and 5 μm (c).



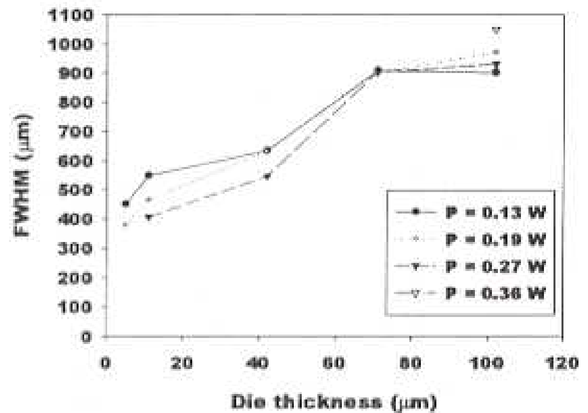


Figure 5. Profile showing the temperature rise along the line S shown in Figure 4c). A Lorentzian distribution is fitted to the left end side of the profile (dotted line).

The full width half maximum (FWHM) value of the Lorentzian fit was calculated for temperature profiles acquired for different die thicknesses and for power dissipations ranging from 130 mW to 360 mW. The FWHM measurements are shown in Figure 6. At the lower thicknesses, measurements at high power were not made to avoid overheating the sample.

The increase in resolution with increasing power dissipation is apparent in Figure 6. However, one does not improve the resolution significantly by using higher powers. The curves of Figure 6 suggest that the most efficient way to improve the resolution is to thin the Si die. Extrapolation of the curves to zero thickness gives a FWHM value of about 350 μm. The fact that the data do not extrapolate through the origin is due to heat dissipation by the underfiller material.

Figure 6. FWHM (along the line S shown in Figure 4c) of the Lorentzian fit to different temperature profiles acquired for different thicknesses and different power dissipations.

The quoted FWHMs are large and might suggest a rather severe limitation of this technique for failure analysis. As mentioned above however, the location of the centroid for a hot spot in failure analysis can be done to within a few micrometers if the die has been sufficiently thinned.

The isotherms represented in Figure 7 were obtained by applying a power of 190 mW on the 5 μm thick Si die. The solder bumps are approximately 400 μm apart. The layout as well as the location of the solder bumps are superimposed in black. The temperature variation between two isotherms is 3 °C. The heat-sinking effect of the solder bumps is evident in this figure. Temperature maps such as the one in Figure 7 can be used to analyze the flow of heat in new designs or in failure analysis.

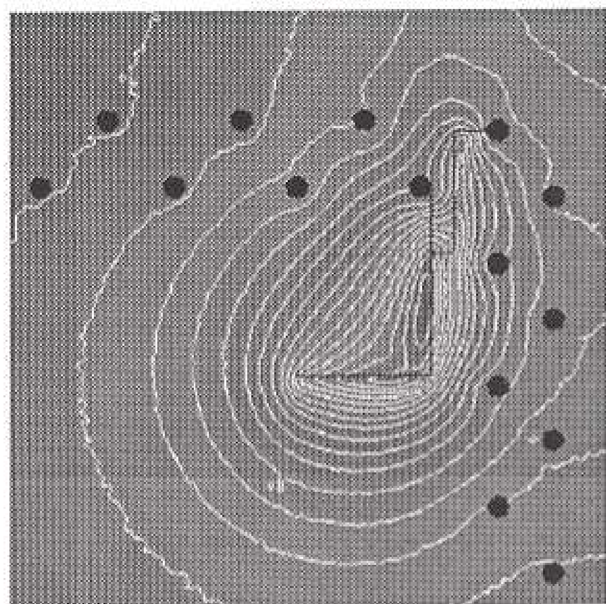


Figure 7. Isotherms showing the heat-sinking effect of the bumps. A schematic of the bumps and of the active circuit is superimposed onto the temperature map. The temperature variation between the lines is of 3 °C.

The heat-sinking effect measured here is not representative of the system's normal dissipation dynamics. The important thinning of the die does change significantly the heat transfer phenomena within the sample. However, those experimental results could allow one to verify 3D numerical models in the limit for a very thin die (5 µm).

IV. Conclusions

We have shown that the analysis of FCOB using FMI is possible, but that it requires significant polishing of the Si die from the backside. Underfilled FCOB's have to be polished down to about 5 µm to obtain a spatial resolution of 50 µm or better. Hot spots, as encountered in failure analysis, can be located within a few micrometers by using the centroid of the thermal profile. Polishing the die to less than 3 µm will likely affect the integrity of the circuitry. Local thinning (under 5 µm) of the die could also be done using the FIB. Then, by repeating FMI in this area a higher resolution is obtained and the exact failure site is more likely to be detected.

A temperature map around the solder bumps of a test circuit was obtained after thinning the die to 5 µm. The map clearly shows that the temperature contours are affected by the presence of the solder bumps which act as important heat sinks.

Acknowledgment

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