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A novel laser trimming technique for microelectronics

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Abstract

A novel laser trimming technique, fully compatible with conventional CMOS processes, is described for analogue and mixed microelectronics applications. In this method, a laser beam is used to create a resistive device by melting a silicon area, thereby forming an electrical link between two adjacent p–n junction diodes. These laser diffusible resistances can be made in less than a second with an automated system, and their values can be in the range 100 Ω to a few megaohms, with an accuracy of 50 ppm, by using an iterative process. In addition, these resistances can also be made to possess a TCR (temperature coefficient of resistance) close to 0. We present the method used to create these resistances, the main device characterization and some insight on process modeling. © 2001 Published by Elsevier Science B.V.

Keywords: Laser trimming; Analogue microelectronics; Resistance

1. Introduction

In spite of the steady progress of digital electronics, nowadays electronic systems often contain significant analogue sub-systems, because their connection to the external world often implies dealing with analogue signals. Actually, the general model of a digital core with analogue external interfaces is found in most telecommunication, digital signal processing and control applications. While the growing transistor counts available with digital integrated circuits that can absorb all functions of many electronic systems, analogue sub-systems get integrated at a much slower pace, due primarily to their component accuracy requirements. For systems that need high accuracy, system designers are usually forced to use some sort of trimming. This may sometimes be avoided by relying on a limited number of high accuracy components, which tend to be relatively expensive, by hiding from the user some sort of interior trimming, or by referring all key performance parameters to a single device that determines system accuracy. For instance, Taylor and Hanlon [1] describe the design of a 12-bit DAC (digital to analogue converter) implemented using wafer laser trimming. In most approaches, trimming involves the modification of the impedance or resistance of integrated components through the use of laser, ion or electron beams [2–14]. The methods based on laser ablation of thin [2,3,6] or thick [4–6] films, mesh trimming [7] and polysilicon link making [8,9] all require an additional process step to deposit the resistive film. Laser polysilicon link making even

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requires masking of the polysilicon film prior to implantation. Polymer trimming [10], in which polymer conductivity is changed by exposition to infrared light, not only requires an additional material layer, but is also very slow. Pulsed voltages [11,12] and floating gate [13] methods present the advantage of compensating for the resistance of the package pins. Even if integrated circuits can be trimmed after packaging, this method requires additional pads to provide the electrical stimulus used to trim, which consumes significant die space, particularly with low pin count analogue or mixed signal components. In most techniques presented above, the additional process steps increase cost and consume significant die area, which limits their flexibility and usefulness.

The method presented in this paper is an extension of the laser-induced diode linking that was originally proposed for wafer-scale integration [15–17]. By a careful iterative approach, this diode linking method is used for impedance tuning of semiconductor resistances. This novel trimming method produces laser diffusible resistances that can be very accurate, uses very small die area, and can be integrated into any existing CMOS process without any additional masking step. A patent disclosing the detailed device structure and creation method has been accepted at the US and Canadian patent offices, and was also submitted as a PCT patent [14].

2. Principle of the laser trimming method and experimental setup

The laser trimming technique is applied to a device structure shown in Fig. 1. Put simply, this structure is a MOSFET with no gate contact, fabricated with any conventional CMOS process. For an n-type resistor, the device structure consists of two highly doped regions, separated by a distance *L*, and formed by implantation into a p-well, resulting into two p–n junctions facing each other. The device has a width *W* and the electrical connections to the structure are formed using contacts. Finally, an oxide layer protects the device. Complementary doping types are used for a p-type resistor. Before performing laser trimming, the only currents that can flow through the device are leakage currents from the p–n junctions to the substrate, resulting essentially in an open circuit. Focusing a laser beam on the gap region between the two junctions melts the silicon, resulting in dopant diffusion from the highly doped regions to the lightly doped gap region. Upon removal of the laser light, the silicon freezes and solidifies, leaving the diffused dopants in a new local distribution, which may form an electrical link between the highly doped regions. This laser-diffused link constitutes the trimmed resistance. Tight control of process parameters is necessary to efficiently create these laser diffusible resistances, while avoiding damage to adjacent devices and structures. These parameters are the laser spot size, pulse duration, laser power, number of laser exposures and position of the laser spot relative to the device. By varying these parameters between each laser irradiation, one can accurately tune the device. The laser trimming system used comprises a Coherent Innova 90 5 W argon ion laser, running all lines for maximum possible power, an acousto-optic modulator (AOM) from Neos technologies implemented as a high-speed shutter, and a Klinger *X*–*Y*–*Z* positioning table. The laser beam is focused on the device structure to a spot 2 μm in diameter, and the system is computer controlled to speed up the process.

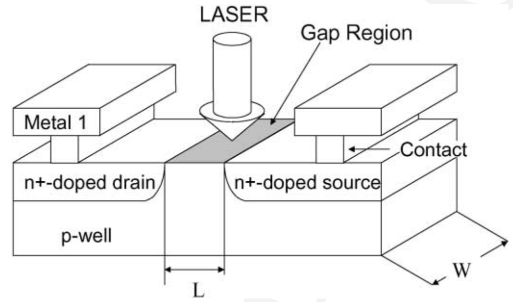

Fig. 1. Schematic cross-section of the laser diffusible resistance.

3. Device characterization

While the results presented here were obtained on devices made with the MITEL 1.5 μm technology with dimensions $L = 1.7$ μm and $W = 6$ μm, we have successfully verified that the method works for a 0.35 μm technology. A large number of laser diffusible resistances, with a 100% yield, have been created using a prototype integrated circuit comprising many target sites on the same circuit.

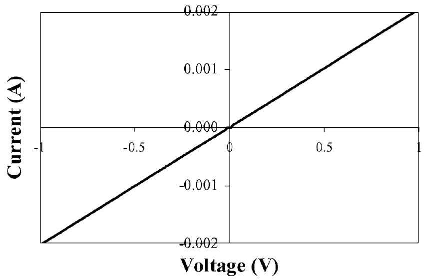

Fig. 2. Typical *I–V* characteristic of a laser diffusible resistance (value = 492 Ω) at room temperature.

Current–voltage characteristics were measured using a Hewlett Packard 4155A semiconductor parameter analyzer. *I–V* characteristics for all devices produced by our iterative laser trimming process show excellent linear behavior at potential differences smaller than 0.3 V. Resistance values from 100 Ω to as high as a few megaohms, with accuracy of 50 ppm, can be made easily. Typical *I–V* characteristic for a 492 Ω device is shown in Fig. 2.

Resistance as a function of temperature was measured using a Hewlett Packard 34401A digital multimeter and a Yamato Scientific America DX300 oven to control the device temperature. Fig. 3 depicts typical resistance variations as a function of temperature. Resistances having values lower than 1.5 kΩ present a positive temperature coefficient, and those with values higher than 3 kΩ present a negative temperature coefficient. For a gap of 1.7 μm and a width of 6 μm, there exists a resistance for which the temperature coefficient is close to 0. This value is around 2 kΩ in this case, and it is expected to vary with device geometry and doping levels.

Fig. 4 shows images produced with an atomic force microscope (AFM) and a scanning capacitance microscope (SCM) (Digital Instruments, Dimension 3100 model) of a laser-diffused resistance, where all outer dielectric layers have been removed by an HF etch. Five laser pulses were used in this experiment and the laser parameters were maintained at 0.75 W (incident on the surface of the chip) and 1 μs duration. While the AFM image reveals no significant deformation of the p-well, the SCM image shows clearly that dopants, as represented by dark gray, have diffused from the two n^+ regions into the p-channel. The diffused region is about 1 μm in size.

4. Process modeling

Modeling this process involved a time-dependent three-dimensional (3D) calculation of the temperature due to the laser irradiation, followed by a dopant distribution calculation using Fick's law. A simple model must include the effects of the laser power, beam waist and exposure time as well as the geometric characteristics of the initial structure. Device characteristics can then be evaluated by solving the three differential coupled equations to obtain the 3D dis-

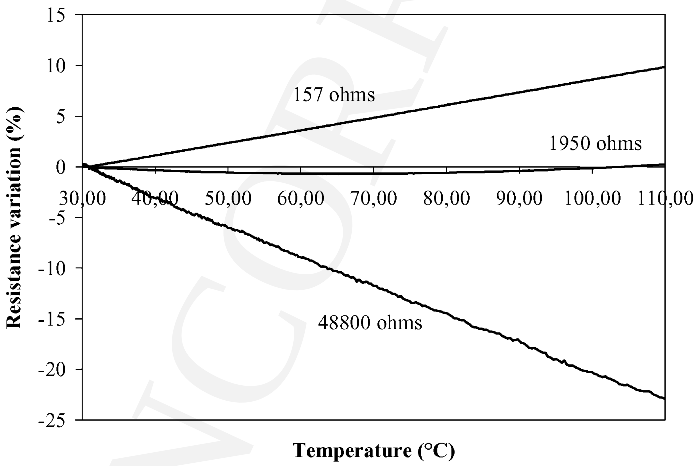

Fig. 3. Resistance variation in percent (relative to the 30 °C value) as a function of temperature for three laser diffusible resistances with nominal values at 30 °C of 157, 1950 and 48 800 Ω.

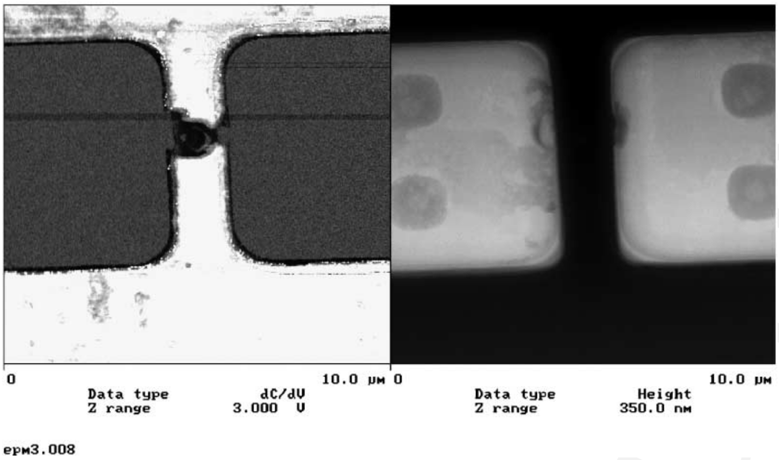

Fig. 4. SCM (left) and corresponding AFM image (right) of diffused resistance. The n-channel is clearly visible on the SCM image, whereas topography (AFM) reveals no significant deformation of the p-well.

tributions of electron and hole concentrations, as well as the electric field in this device presenting a non-uniform dopant distribution. In addition, modeling must also include the possibility of varying the laser beam location and power from pulse to pulse to obtain the desired device characteristics.

Some insight on process modeling can be obtained by using careful approximations. We consider the effect of a focused laser beam incident on an n^+–p–n^+ silicon structure, resulting in the diffusion of dopants into silicon. Because the diffusion length of dopants in liquid Si is 4 orders of magnitude higher than that of crystalline Si [19], we assume that only dopants in the silicon melt diffuse. During the laser pulse, the silicon melt dimension increases and then decreases as the pulse ends. Therefore, we propose that only the *maximum* melted region (as denoted by r_{melt} on the Si surface) has to be determined in the temperature calculation; the dopants located outside this region are assumed to be immobile. As the pulse duration t increases, dopants with a diffusion coefficient D will have more time to diffuse over a length of $r_D = 2\sqrt{Dt}$ in the entire melted region yielding a more uniform dopant distribution. For instance, arsenic ($D = 3.3 \times 10^{-4}\,\mathrm{cm^2/s}$ in liquid Si [19]) was the major dopant in the n^+ regions of the structures investigated and $r_D\,(\mathrm{m}) = 0.4\sqrt{t\,(\mathrm{s})}$, suggesting that laser pulses of a few microseconds are required for uniform dopant distribution over a fraction of a micrometer.

The calculation of the temperature distribution resulting from a focused laser beam is based on a method by Bäuerle [18] and Cohen et al. [16]. The heat diffusion equation is solved in the case of a Gaussian beam of radial symmetry and exponentially decaying optical absorption. The pulse is rectangular in time. The temperature dependence of the thermal conductivity is taken into account via a Kirchhoff transformation. The solution of this problem is in the form of a temporal integral to be solved numerically. In the method proposed by Cohen et al., optical absorption and heat diffusion coefficient do not vary with temperature. Furthermore, the latent heat of fusion is not incorporated into the calculations and only the steady state problem is solved (though it is pointed out that the solution of the time-dependent problem can be obtained merely by changing the integration limits).

We extend Cohen's method to the time-dependent problem, including latent heat of fusion and partially taking into account temperature-dependent reflectivity, optical absorption and heat diffusion coefficient. This is done within an adiabatic approximation [20] where the time evolution of the temperature can be monitored by separating the time integral into small segments. After each temperature increment, the silicon properties are adjusted to the new temperature before the next temperature jump is calculated. In this way, the important variation of silicon properties as a function of temperature, particularly at the solid/liquid transition, are partially included. As for the latent heat of fusion,

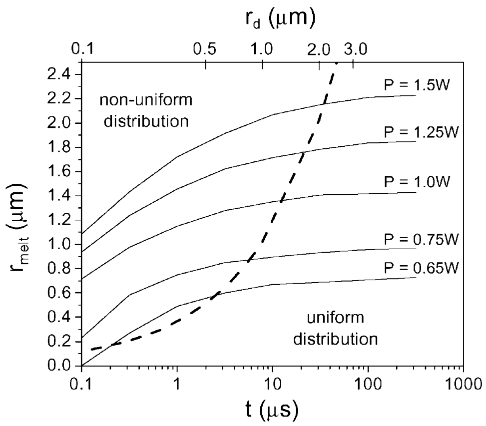

Fig. 5. Maximum silicon melt radius r_{melt} as a function of pulse duration t and laser power. Laser $1/e$ radius is 1.0 μm. The dashed line separates the uniform dopant distribution from the non-uniform distribution.

an internal loop in the numerical algorithm insures that it is taken into account. When the temperature reaches the melting point (T_f), it is maintained at this value and the subsequent temperature rises are converted into enthalpy until sufficient energy is accumulated [21], i.e. when the enthalpy of silicon reaches the latent heat of fusion. The next temperature calculations are then made as before, with the exception that the material properties are those of liquid silicon.

Fig. 5 shows the results of numerical calculations of r_{melt} as a function of laser duration for different laser powers at a fixed waist of 1.0 μm. For a laser power of 0.75 W and 1 μs, the calculation is in relatively good agreement with the SCM results of Fig. 4. In addition, conditions for uniform dopant distribution are located on the right side of the dashed line corresponding to $r_{melt} = r_D$. Fig. 5 can then be used to determine the laser power and time width t of the various laser exposures in an iterative process to fine-tune the dopant distribution to yield a specific resistance value.

5. Conclusion

Laser diffusible resistances can be made accurately by an iterative process to obtain resistance values between 100 Ω and a few megaohms. This new trimming technique is compatible with CMOS processes and can accurately produce resistances in less than a second. Further studies are being performed on process optimization and modeling, as well as on applications of these resistances in analogue microelectronic circuits. These studies will be the subjects of future publications. This technique is being implemented for high-volume production of integrated circuits by LTRIM technologies.

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