LASER TUNNING SILICON MICRODEVICES FOR ANALOG MICROELECTRONICS

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ABSTRACT

A novel laser tunning technique, fully compatible with conventional CMOS processes, is described for analog and mixed microelectronics applications. In this method, a laser beam is used to create a resistive device by melting a silicon area, thereby forming an electrical link between two adjacent p-n junction diodes. These laser diffusible resistances can be made in the range of 100Ω to a few MΩ, with an accuracy of 50ppm, by using an iterative process

INTRODUCTION

In spite of the steady progress of digital electronics, nowadays electronic systems often contain significant analogue sub-systems, because their connection to the external world often implies dealing with analog signals. Actually, the general model of a digital core with analog external interfaces is found in most telecommunication, digital signal processing and control applications. While the growing transistor counts available with digital integrated circuits allow absorbing all functions of many electronic systems, analog subsystems get integrated at a much slower pace, due primarily to their component accuracy requirements. For systems that need high accuracy, system designers are usually forced to use some sort of trimming. This may sometimes be avoided by relying on a limited number of high accuracy components, which tend to be relatively expensive, by hiding to the user some sort of trimming inside, or by referring all key parametric performances to a single device that determines system accuracy. For instance, Taylor and Hanlon describe the design of a 12-bit DAC (Digital to Analog Converter) implemented using wafer laser trimming[1]. In most approaches, trimming involves the modification of the impedance or resistance of integrated components through the use of laser, ion or electron beams[2-14]. The methods based on laser ablation of thin[2-3, 6] or thick[4-5, 6] films, mesh trimming[7] and polysilicon link making[8-9] all require an additional process step to deposit the resistive film. Laser polysilicon link making even requires masking of the polysilicon film prior to implantation. Polymer trimming[10], which consists of a change in the polymer conductivity by its exposition to infrared light, not only requires an additional layer, but is also very slow. Pulsed voltages[11-12] and floating gate[13] methods present the advantage of compensating for the resistance of the package pins. Even if integrated circuits can be trimmed after packaging, this method requires additional pads to provide the electrical stimulus used to trim, which consumes significant die space, particularly with low pin count analog or mixed signal components. In most techniques presented above, the additional process steps increase cost and consume significant die area, which limits their flexibility and usefulness.

The method presented in this paper is an extension of the laser-induced diode linking that was originally proposed for wafer-scale integration[15-16-17]. By a careful iterative approach, this diode linking method is used for impedance tuning of semiconductor resistances. This novel trimming method produces laser diffusible resistances that can be very accurate, uses very small die area, and can be integrated into any existing CMOS process without any additional masking step. A patent disclosing the detailed device

structure and creation method has been accepted at the US and Canadian patent offices, and was also submitted as a PCT patent[14].

PRINCIPLE OF THE LASER TRIMMING METHOD

The laser tunning technique is applied to a device structure shown in Fig. 1. Put simply, this structure is a MOSFET with no gate, fabricated with any conventional CMOS process. For an n-type resistor, the device structure consists of two highly doped regions, separated by L, and formed by implantation into a p-well, resulting into two p-n junctions facing each other. The device has a width W and the electrical connections to the structure are formed using contacts. Finally, an oxide layer protects the device. Complementary doping types are used for a p-type resistor. Before performing laser tunning, the only currents that can flow through the device are leakage currents from the p-n junctions to the substrate, resulting essentially in an open circuit. Focusing a laser beam on the gap region between the two junctions causes melting of the silicon, resulting in dopant diffusion from the highly doped regions to the lightly doped gap region. Upon removal of the laser light, the silicon freezes and solidifies, leaving the diffused dopants in a new local distribution, which may form an electrical link between the highly doped regions. This laser-diffused link constitutes the tunned resistance. Tight control of process parameters is necessary to create efficiently these laser diffusible resistances, while avoiding damage to adjacent devices and structures. These parameters are the laser spot size, pulse duration, laser power, number of laser expositions and position of the laser spot relative to the device. By varying these parameters between each laser irradiation, one can accurately tune the device. The laser trimming system used comprises a Coherent Innova 90 5W Argon ion laser, running all lines for maximum possible power, a high-speed shutter implemented as an acousto-optic modulator (A.O.M.) from Neos Technologies, and a Klinger X-Y-Z positioning table. The laser beam is focused on the device structure to a spot 2µm in diameter, and the system is computer controlled to speed up the process.

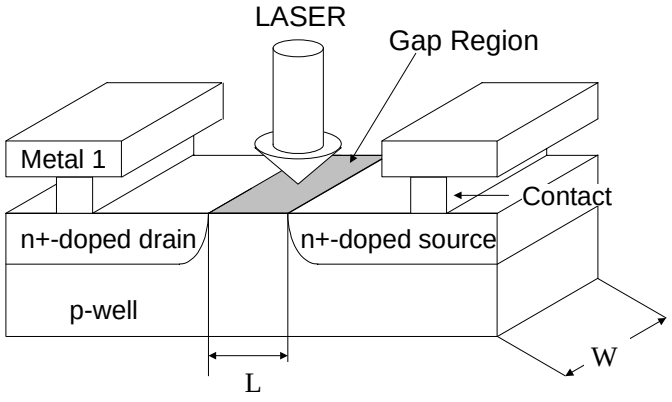

Fig. 1 Schematic cross section of the laser diffusible resistance.

RESULTS

While the results presented here were obtained on devices made on the MITEL 1.5µm technology with dimensions L=1.7µm and W= 6µm, we have successfully verified that the method works for a 0.35µm technology. A large number of laser diffusible resistances, with a 100% yield, have been created using a prototype integrated circuit comprising many target sites on the same circuit. Current-voltage characteristics have been measured using a Hewlett Packard 4155A semiconductor parameter analyzer. I-V characteristics for all devices produced by our iterative laser tunning process show excellent linear behavior at potential differences smaller than 0.3V. Resistance values from 100Ω to as high as a few MΩ, with accuracy of 50ppm, can be made easily. Typical I-V characteristic for a 492.0 Ω device is shown in Fig. 2.

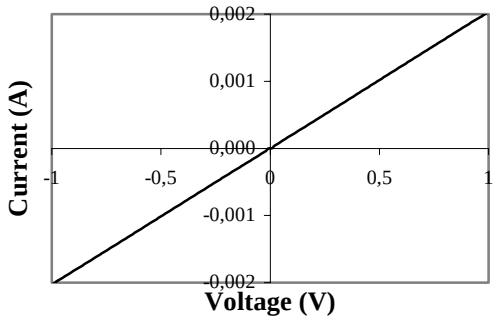

Fig. 2: Typical I-V characteristic of a laser diffusible resistance (value = 492.0 Ω) at room temperature.

CONCLUSION

In conclusion, laser diffusible resistances can be made accurately by an iterative process to obtain resistance values between 100Ω and a few MΩ. This new tunning technique is compatible with CMOS processes. Further studies are being performed on applications of these resistances in analog microelectronic circuits. This technique is being implemented for high volume production of integrated circuits by LTRIM Technologies.

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