A novel laser trimming technique for microelectronics

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ABSTRACT

A novel laser trimming technique, fully compatible with conventional CMOS processes, is described for analogue and mixed microelectronics applications. In this method, a laser beam is used to create a resistive device by melting a silicon area, thereby forming an electrical link between two adjacent p-n junction diodes. These laser diffusible resistances can be made in less than a second with an automated system and their values can be in the range of 100Ω to a few MΩ, with an accuracy of 50ppm, by using an iterative process. In addition, these resistances can also be made to possess a thermal coefficient close to zero. We present the method used to create these resistances, the main device characterization and some insight on the process modeling.

Keywords: Laser trimming, analogue microelectronics, resistance

1- INTRODUCTION

In spite of the steady progress of digital electronics, nowadays electronic systems often contain significant analogue sub-systems, because their connection to the external world often implies dealing with analogue signals. Actually, the general model of a digital core with analogue external interfaces is found in most telecommunication, digital signal processing and control applications. The strong push toward System on Chip (SoC) increases the pressure to raise the integration level of analogue components, and at maturity allows implementing sophisticated monolithic SoC comprising all digital and analogue electronic components. While the growing transistor counts available with digital integrated circuits allow absorbing all functions of many electronic systems, analogue subsystems get integrated at a much slower pace, due primarily to their component accuracy requirements. Some of the methods used by system designers to deal with this issue include referring everything to a crystal frequency, using accurate resistor ladders with excellent matching and stability properties, and trimming with a potentiometer. Some of these techniques are used at the integrated circuit level. For instance, analogue components are very often designed using components whose relative parametric properties are well matched, even though they are not very accurate in absolute terms. Another technique is to use a digitally controlled potentiometer, which includes an analogue to digital converter that typically relies on matched transistors or matched resistors. With state-of-the-art practices, 8-bit accuracy is typically obtained with parallel digital to analogue converters (DAC). For systems that need better accuracy, system designers are usually forced to use some sort of trimming. This may sometimes be avoided by adopting a limited number of high accuracy components, which tend to be very expensive and hide to the user some sort of trimming inside or by referring all key parametric performances to a single device that limits processing throughput. For instance, Taylor and Hanlon describe the design of a 12-bit DAC implemented using wafer laser trimming[1].

Table 1 summarizes some major resistance trimming techniques that are crucial for the development of analogue microelectronics. In most approaches, trimming involves the modification of the impedance or resistance of integrated components through the use of laser, ion or electron beams[2-14]. The methods based on laser ablation of thin or thick films, mesh trimming and polysilicon link making all require an additional process step to deposit the resistive film. Laser polysilicon link making even requires masking of the polysilicon film prior to implantation. Polymer trimming, which consists of a change in the polymer conductivity by its exposition to infrared light, not only requires an additional layer, but is also very slow. Pulsed voltages and floating gate methods present the advantage of compensating for the resistance of the package pins. Even if integrated circuits can be trimmed after packaging, this method requires additional pads to provide the electrical stimulus used to trim, which consumes significant die space, particularly with low pin count analog or mixed signal components. In most techniques presented above, the additional process steps increase cost and consume significant die area, which limits their flexibility and usefulness.

The method presented in this paper is based on the laser-induced diode linking that has already been proposed for wafer-scale integration[15-16]. By a careful iterative approach, this diode linking method is used for impedance tuning of semiconductor resistances. This novel trimming method produces laser diffusible resistances that can be very accurate, uses very small die area, and can be integrated into any existing CMOS process without any additional masking steps. A patent disclosing the detailed device structure and creation method is pending at the US and Canadian patent offices and it has also been submitted as a PCT patent[14].

Table 1: Major resistance trimming methods

Method	**Resolution**	**Size**	**Special Processing (besides trimming)**
Thin[2-3] and thick[4-5] film trimmed by laser, ion beam and electron beam[6]	Continuous	Large	Resistive film
Mesh trimming[7]	Discontinuous	Large	Resistive film
Laser polysilicon link making[8-9]	Continuous	Small	Polysilicon film on field oxide with masking and implantation
Polymer trimming[10]	Continuous	Large	Polymer film
Pulsed voltage[11-12]	Continuous	Large	Resistive film and additional pads
Floating gate device[13]	Continuous	Large	Additional pads
Laser-diffused resistance[14]	Continuous	Very small	None

2- PRINCIPLE OF THE LASER TRIMMING METHOD

The laser trimming technique is performed on a device structure shown in figure 1, consisting of a MOSFET with no gate fabricated by any conventional CMOS process. For an n-type resistor, the device structure consists of two highly doped regions, separated by L and formed by implantation into a p-well, resulting into two p-n junctions facing each other. The device has a width W and the electrical connections to the structure are formed using contacts. Finally, an oxide layer protects the device. Complementary doping types are used for a p-type resistor. Before performing laser trimming, the only currents that can flow through the device are leakage currents from the p-n junctions to the substrate, resulting essentially in an open circuit.

Focusing a laser beam on the gap region between the two junctions causes melting of the silicon, resulting in dopant diffusion from the highly doped regions to the lightly doped gap region. Upon removal of the laser light, the silicon freezes and solidifies, leaving the diffused dopants in a new local distribution, forming an electrical link between the highly doped regions. This laser-diffused link constitutes the trimmed resistance. Tight control of process parameters is necessary to create efficiently these laser diffusible resistances, while avoiding damage to adjacent devices and structures. These parameters are the laser spot size, pulse duration, laser power, number of laser expositions and position of the laser spot relative to the device. By varying these parameters between each laser irradiation, one can accurately tune the device.

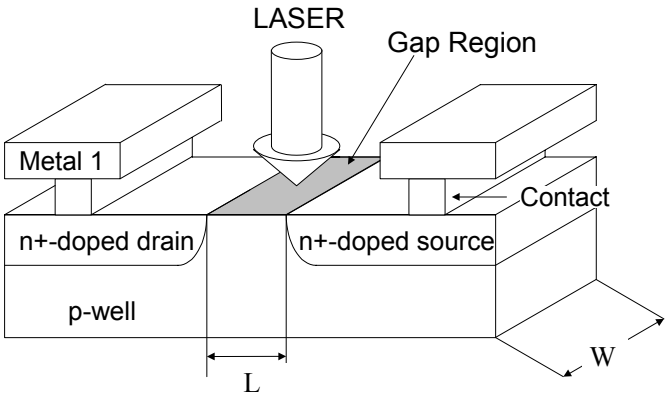

Figure 1 Schematic cross section of the laser diffusible resistance.

3- EXPERIMENTAL SETUP

Fig 2 shows schematically the laser trimming system used to create these links. We used a Coherent Innova 90 5W Argon ion laser, running all lines for maximum possible power, as the local heat source for melting the silicon. A Neos Technologies acousto-optic modulator was used as a high-speed shutter. A Hewlett Packard 81101A pulse generator provides the modulation signal to control the acousto-optic modulator. The laser beam is focused on the device structure to a spot 2µm in diameter by a microscope objective manufactured by Mitutoyo. A Klinger X-Y-Z positioning table consisting of a stacking of 3 stepping motor translation stages performed positioning of the device relative to the laser beam. The X and Y-axis provide motion normal to the incident beam and the Z-axis is used to position the device vertically, with 1µm resolution, so that the spot size can be adjusted precisely. An Hitachi CCD camera allows visualization of the device on the trimmed integrated circuit via a mirror that can be removed during laser interventions. The system is controlled by a computer to speed up the process.

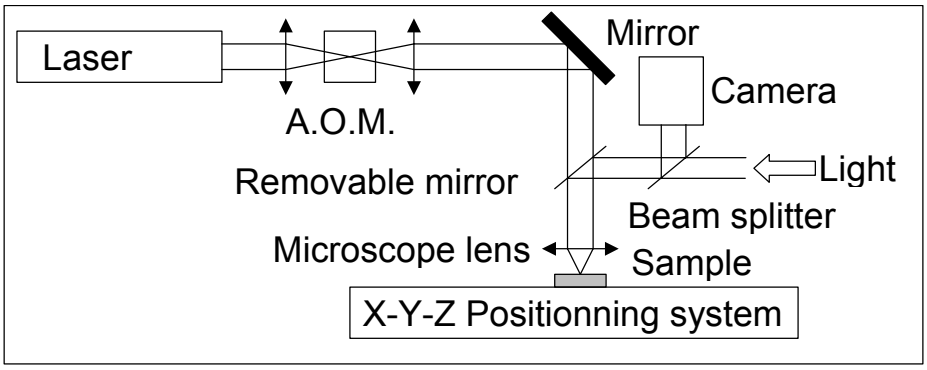

Figure 2 Schematic of the laser trimming system.

4- DEVICE CHARACTERIZATION

While the results presented here were obtained on devices made on the MITEL 1.5µm technology with dimensions L=1.7µm and W= 6µm, we have successfully verified that the method works for a 0.35µm technology. A large number of laser diffusible resistances, with a 100% yield, have been created using a prototype integrated circuit comprising many target sites on the same circuit.

Current-voltage characteristics have been measured using a Hewlett Packard 4155A semiconductor parameter analyzer. I-V characteristics for all devices produced by our iterative laser trimming process show excellent linear behavior at potential differences smaller than 0.3V. Resistance values from 100Ω to as high as a few MΩ with accuracy of 50ppm can be made easily. Typical I-V characteristic for a 492Ω device is shown in figure 3.

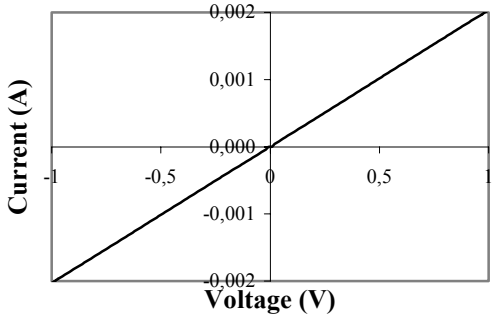

Figure 3: Typical I-V characteristic of a laser diffusible resistance (value = 492Ω) at room temperature.

For all devices, after the linear relation at low voltages, a sub linear behavior at intermediate voltages followed by an exponential increase at higher voltages are observed as the potential difference increases. This is shown in figure 4 for a 10kΩ resistance. These non-linear behaviors are obtained for all devices; only the voltage ranges for the different behaviors vary depending on the resistance values. Indeed, as the resistance value increases, the non-linear effects are observed at lower voltages. This behavior is indicative of the influence of the dopant distribution on the I-V characteristics. For low resistance values, the dopants probably approach a uniform distribution, leading to a uniform field < $5x10^3$V/cm (1 V over $2x10^{-4}$ cm), corresponding to the onset of non-linear behavior on the mobility[17]. For higher resistance values, dopants probably exhibit a non-uniform distribution, leading to a region of higher resistive value supporting higher fields at even lower voltages. In all devices, at still higher voltages, non-linear behavior due to band bending effects is also observed, as seen in figure 4 for V>3V. These results indicate that to obtain a more linear resistance over a larger voltage range, one has to create a laser-diffused resistance with a more uniformly doped region, to lower the local electric fields.

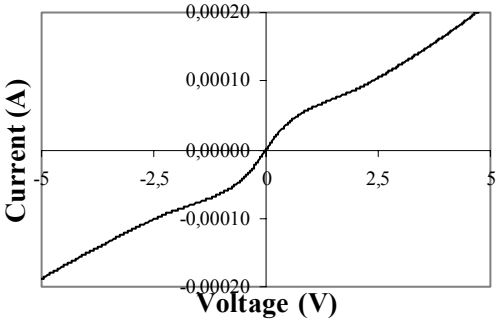

Figure 4 :Typical I-V characteristics of a 10kΩ resistance at room temperature, showing non-linear effects at high voltages.

Resistance as a function of temperature has been measured using a Hewlett Packard 34401A digital multimeter and a Yamato Scientific America DX300 oven to control the device temperature. Fig 5 depicts typical resistance variations as a function of temperature. Resistances having values lower than 1.5kΩ present a positive temperature coefficient and those with values higher than 3kΩ present a negative temperature coefficient. For a gap of 1.7µm and a width of 6µm, there exists a

resistance for which the temperature coefficient is close to zero. This value is around 2kΩ in this case and is expected to vary with device geometry and doping levels.

A detailed analysis of the I-V characteristics as a function of voltage and temperature will be the subject of another publication.

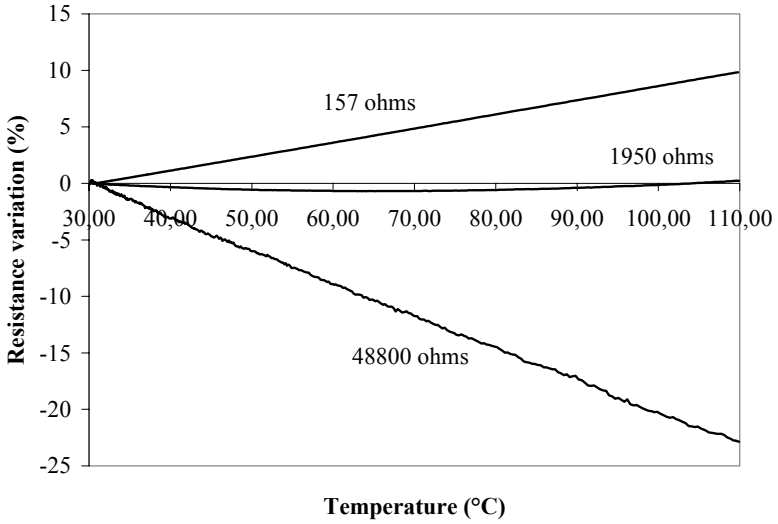

Figure 5: Resistance variation in percent (relative to the 30°C value) as a function of temperature for three laser diffusible resistances with nominal values at 30°C of 157Ω, 1950Ω and 48800Ω.

5- PROCESS MODELING

Modeling this process involved a time dependant three-dimensional (3D) temperature calculation, due to the laser irradiation followed by a dopant distribution calculation using Fick's laws. A basic model must include the effects of the laser power, waist and time duration as well as the geometric characteristics of the initial structure. Device characteristics can then be evaluated by solving the three differential coupled equations to obtain the 3D distributions of electron and hole concentrations, as well as the electric field in this device presenting a non-uniform dopant distribution. In addition, modeling must also include the possibility of varying the laser beam location and power from pulse to pulse to obtain the desired device characteristics.

Some insight on process modeling can be obtained by using careful approximations. We consider the effect of a focused laser beam incident on a n^+-p-n^+ silicon structure, resulting in the diffusion of dopants into silicon. Because the diffusion length of dopants in liquid Si is four orders of magnitude higher than that of crystalline Si[18], we assume that only dopants in the silicon melt diffuse. During the laser pulse, the silicon melt dimension increases and then decreases as the pulse ends. Therefore, we propose that only the *maximum* melted region (as denoted by r_{melt} on the Si surface) has to be determined in the temperature calculation; the dopants located outside this region are supposed to be immobile. As the pulse time width t gets longer, dopants with a diffusion coefficient D will have more time to diffuse over a length of $r_D = 2\sqrt{Dt}$ in the entire melted region, yielding to a more uniform dopant distribution. For instance, Arsenic ($D=3{,}4\times10^{-4}cm^2/s$ in liquid Si[18]) was the major dopant in the n^+ regions of the structures investigated and $r_D(\mu m) = 0.4\sqrt{t(\mu s)}$, suggesting that laser pulses of a few microseconds are required for uniform dopant distribution over a fraction of a micrometer.

The calculation of the temperature distribution resulting from a focused laser beam is based on the paper by Cohen et al.[15]. The heat diffusion equation is solved in the case of a Gaussian beam of radial symmetry and the reflectivity is considered constant and taken at room temperature (R=0,37 for λ = 514nm[19]). Optical absorption is limited to the surface and thermally dependent thermal conductivity is taken into account via a Kirchhoff transformation. The resulting equation is solved numerically with Matlab to determine the liquid-solid boundary. Figure 6 shows the r_{melt} as a function of laser pulse time width for different laser powers at a fixed waist of 1.0μm. Conditions for uniform dopant distribution are located on the right side of

the dashed line corresponding to $r_{melt} = r_D$. Figure 6 can then be used to determine the laser power and time width t of the various laser expositions in the iterative process to fine control the dopant distribution yielding to a specific resistance value.

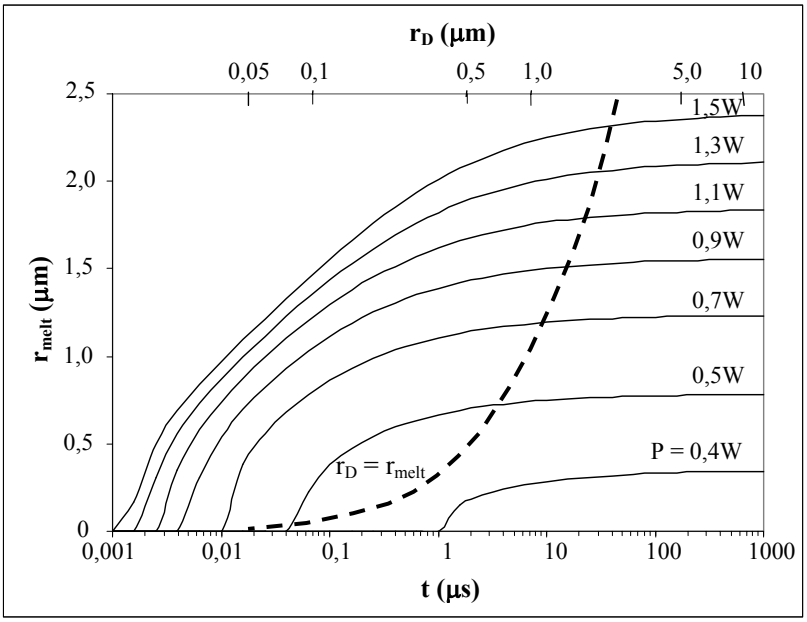

Figure 6: Melt radius r_{melt} as a function of pulse time width t for different laser powers. The laser beam waist is 1.0μm. The dashed line, which corresponds to the condition $r_{melt} = r_D$, separates the uniform dopant distribution on its right side from the non-uniform distribution.

Resistance value can be estimated by assuming that laser conditions are such that in each pulse, the dopants distribute uniformly over the melted regions. By varying the laser power and the laser position, various overall shapes of melted regions can be formed. As an example, figure 7 shows a special condition in which three laser pulses of identical characteristics along a line between the n+ regions give an n channel with an "almost" rectangular shape at its surface. We consider the dopant distribution in the n channel to be uniform, all dopants with an average concentration N_D are coming from the n+ regions that overlap on a surface S with the laser pulse. The width of this rectangle is taken to be twice the radius of the silicon melt r_{melt} and its depth is considered constant and equal to z = 0,3μm, the depth of the n+ regions. In this example, we choose r_{melt}=0.85μm corresponding to the minimum required melted region for joining the two n+ regions separated by L=1.7μm. The resistance can then be calculated with $R = d/\sigma A$ where d is the length of the channel (approximated by $L + S/r_{melt}$), A its cross-section (width $2r_{melt}$ =1.7μm and depth z =0.3μm) and σ the conductivity of the channel which depends on N_D. After the first laser pulse in the center of the channel, the second and third laser expositions located at r_d from the center are used to distribute more dopants into the channel. Figure 8 illustrates the importance of the beam position by plotting the resistance as a function of the position of the closest laser pulse to the n+ regions (r_d) . This simplified example shows the possibility to obtain a large range of resistance values by this technique. Experimentally, more laser expositions with lower power are used to fine tune the resistance value in an iterative process.

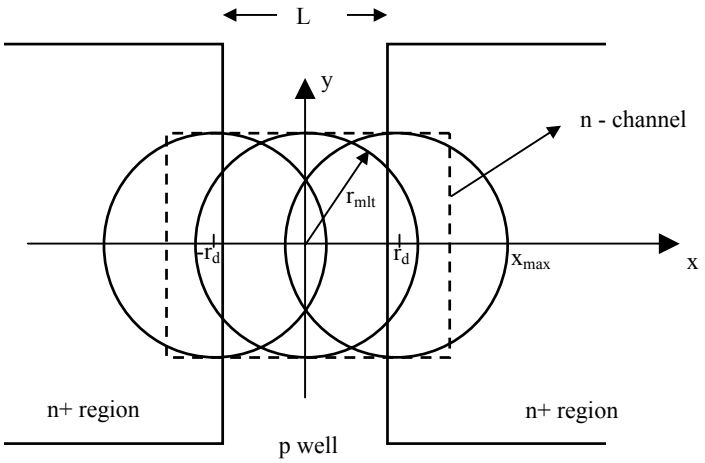

Figure 7: Geometry of a typical laser diffusible resistance. Three identical laser pulses are used, with a spacing of r_d between each.

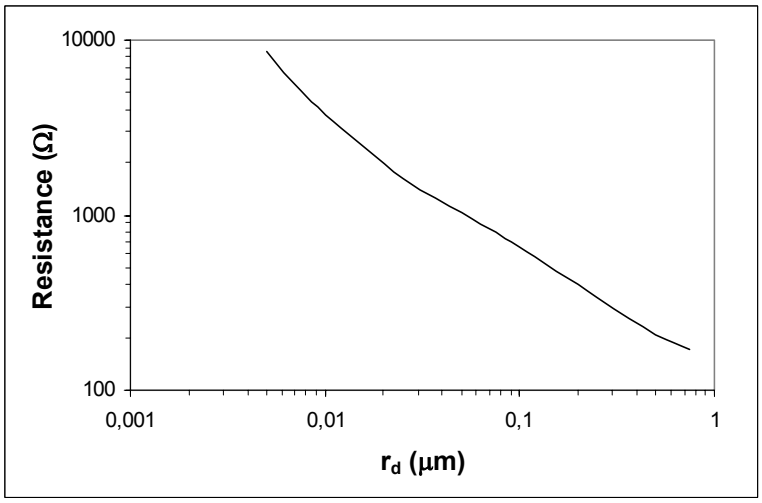

Figure 8: Resistance variation as a function of laser position on the structure r_d as defined in figure 7. The laser characteristics are such that the melt radius r_{melt} is 0,85μm.

6- CONCLUSIONS

Laser diffusible resistances can be made accurately by an iterative process to obtain resistance values between 100Ω and a few MΩ. This new trimming technique is compatible with CMOS processes and can accurately produce resistances in less than a second. Further studies are being performed on the process optimization and modeling as well as on applications of these resistances in analogue microelectronic circuits. These will be the subjects of future publications. This technique is being implemented for high volume production of integrated circuits by LTRIM Technologies.

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